IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	) Examiner: Bowers, Brandon
Deshanand P. Singh, et al.	) Art Unit No. 2825
Application No.: 10/806,617	)
Filed: June 24, 2004	)
For: METHOD AND APPARATUS FOR PERFORMING LOGIC REPLICATION IN FIELD PROGRAMMABLE GATE ARRAYS	)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. 1.131

As the below-named inventors, we declare as follows:

1. We are inventors of the invention described and claimed in the above-identified patent application and of the subject matter described and claimed therein. All acts hereunder took place in the United States, a NAFTA country, or a WTO member country.
2. We are providing this declaration to antedate the reference "Timing Optimization of FPGA Placement by Logic Replication" by Beraudo et al. ("Beraudo"), published June 2-6, 2003, and "Temporal Logic Replication for Dynamically Reconfigurable FPGA Partitioning" by Mak et al. ("Mak"), published July 2003 as cited by the Examiner in the Office Action mailed October 6, 2006.
3. Prior to June 2, 2003, we had completed our invention as described and claimed in at least claims 1-34 of the subject application in the United States, a NAFTA country, or a WTO member country.
4. Attached to this Declaration as Exhibit A is a redacted header file which includes source code. This file was authored by at least one or more of the inventors of the

above-identified patent application prior to June 2, 2003. This file describes an embodiment of the invention as reduced to practice and claimed in at least claims 1-34 of the above-identified patent application. Dates, data structures, and internal comments have been removed in this redacted header file. The date redacted from Exhibit A is prior to June 2, 2003.

5. Prior to June 2, 2003, the inventions of at least claims 1-34 were sufficiently tested to determine and confirm proper operation. The subject matter disclosed in header file and recited in claims 1-34 was executed by a computer or other processing device prior to the publication date of Beraudo and Mak.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements are the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First/Joint Inventor Deshanand P. Singh

Inventor's Signature _____ Date Jan 30, 2007

Full Name of Second/Joint Inventor Gabriel Quan

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